

SYLLABUS/
CURRICULUM



PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

(Approved by AICTE & Affiliated to Anna University, Chennai)

Madurai - Sivagangai Highway, Arasanoor, Thirumansolai Post, Sivagangai Dt. - 630 561, Tamilnadu
Mobile : 9842102628, 7373002628 Email: info@psyec.edu.in Website : www.psyec.edu.in

City Office : 10, Pandian Saraswathi St, Sivagami Nagar, Narayanapuram, Madurai - 625 014. Telefax- 0452 2682338, Mobile : 98423-02628

Department of Electrical And Electronics Engineering

Academic Year 2019-2020

OBJECTIVE OF THE COURSE

- Understand the fundamentals of embedded systems and real-time programming.
- Learn the syntax and semantics of VHDL.
- Develop skills to design, simulate, and implement digital systems using VHDL.
- Gain practical experience with Xilinx FPGA tools and hardware.
- Apply real-time programming concepts in the context of embedded systems.

CHAPTER 1: Introduction to Embedded Systems-Overview of embedded systems-Components of embedded systems-Applications and case studies

CHAPTER 2: Real-Time Systems Fundamentals-Definition and characteristics of real-time systems-Types of real-time tasks-Scheduling algorithms

CHAPTER 3: VHDL Basics-VHDL history and applications-VHDL syntax and structure-Data types, operators, and attributes-Concurrent vs. sequential statements

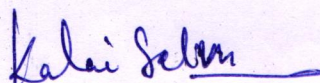
CHAPTER 4: VHDL Design Units-Entity and architecture-Signal and variable declarations-Behavioral, dataflow, and structural modeling

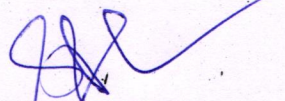
CHAPTER 5: Simulation and Synthesis with VHDL-Testbenches and simulation-Introduction to synthesis-Constraints and optimization- Xilinx FPGA Architecture and Tools-Overview of Xilinx FPGA architecture-Xilinx development tools (Vivado, ISE)-FPGA design flow

OUTCOMES:

- Develop skills to design, simulate, and implement digital systems using VHDL.
- Gain practical experience with Xilinx FPGA tools and hardware.
- Apply real-time programming concepts in the context of embedded systems.

Total: 35 hours


Course Coordinator


HOD/EEE


PRINCIPAL



PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

(Approved by AICTE & Affiliated to Anna University, Chennai)

Madurai - Sivagangai Highway, Arasanoor, Thirumansolai Post, Sivagangai Dt. - 630 561, Tamilnadu
Mobile : 9842102628, 7373002628 Email: info@psyec.edu.in Website : www.psyec.edu.in

City Office : 10, Pandian Saraswathi St, Sivagami Nagar, Narayanapuram, Madurai - 625 014. Telefax- 0452 2682338, Mobile : 98423-02628

Department of Electrical And Electronics Engineering

Academic Year 2019-2020

VACEE1920ESR- Embedded System and Real Time Programming VHDL Program using Xilinx

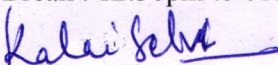
Course Schedule

Date	Time	TOPICS
02/06/2020	9.00 am to 12.30 pm	Introduction to Embedded Systems -Overview of embedded systems-Components of embedded systems-Applications and case studies
	1.00 pm to 5.00 pm	
03/06/2020	9.00 am to 12.30 pm	Real-Time Systems Fundamentals -Definition and characteristics of real-time systems-Types of real-time tasks-Scheduling algorithms
	1.00 pm to 5.00 pm	
04/06/2020	9.00 am to 12.30 pm	VHDL Basics -VHDL history and applications-VHDL syntax and structure-Data types, operators, and attributes-Concurrent vs. sequential statements
	1.00 pm to 5.00 pm	
05/06/2020	9.00 am to 12.30 pm	VHDL Design Units -Entity and architecture-Signal and variable declarations-Behavioral, dataflow, and structural modeling
	1.00 pm to 5.00 pm	
06/06/2020	9.00 am to 12.30 pm	Simulation and Synthesis with VHDL -Testbenches and simulation-Introduction to synthesis-Constraints and optimization- Xilinx FPGA Architecture and Tools-Overview of Xilinx FPGA architecture-Xilinx development tools (Vivado, ISE)-FPGA design flow
	1.00 pm to 5.00 pm	

Total Hours 35

Tea Break : 10:40 am to 10:55am & 02:45 pm to 15:00 pm

Lunch Break : 12:30pm to 01:00pm


Course Coordinator


HOD/EEE


PRINCIPAL



PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

(Approved by AICTE & Affiliated to Anna University, Chennai)

Madurai - Sivagangai Highway, Arasanoor, Thirumansolai Post, Sivagangai Dt. - 630 561, Tamilnadu
Mobile : 9842102628, 7373002628 Email: info@psyec.edu.in Website : www.psyec.edu.in

City Office : 10, Pandian Saraswathi St, Sivagami Nagar, Narayanapuram, Madurai - 625 014. Telefax- 0452 2682338, Mobile : 98423-02628

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Academic Year 2019-2020

One page Report

Name of the course : Embedded System and Real Time Programming VHDL
Program using Xilinx
Development Course Code : VACEE1920ESR
Course Coordinator : Mrs.K KALAISELVI
Date/Duration : 02.06.20-06.06.20— 35 hours

I here affirm that the Third and Final Year students of strength 33 have been taught the value-added course title “**Embedded System and Real Time Programming VHDL Program using Xilinx**” as per the syllabus and completed within the stipulated time duration.

I confirm that the value-added course titled “**Embedded System and Real Time Programming VHDL Program using Xilinx**” has been conducted in the beginning of the semester and course delivery along with the attendance of the students was recorded.

I confirmed that all the students were actively participated in the course and the eligible students were certified for the course.

Mr.K.KalaiSelvi,

AP/EEE

Course Co-Ordinator

Mrs.S.Pandimeena,

AP/EEE

Head of the Department

Principal

Dr. R. RAJA M.E., Ph.D.,
PRINCIPAL
PANDIAN SARASWATHI YADAV
ENGINEERING COLLEGE
Arasanoor, Thirumansolai P.O-630 561
Sivagangai Dist, Tamil Nadu

ASSESSMENT PROCEDURE



PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

(Approved by AICTE & Affiliated to Anna University, Chennai)

Madurai - Sivagangai Highway, Arasanoor, Thirumansolai Post, Sivagangai Dt. - 630 561, Tamilnadu
Mobile : 9842102628, 7373002628 Email: info@psyec.edu.in Website : www.psyec.edu.in

City Office : 10, Pandian Saraswathi St, Sivagami Nagar, Narayanapuram, Madurai - 625 014. Telefax- 0452 2682338, Mobile : 98423-02628

Department of Electrical And Electronics Engineering

Academic Year 2019-2020

VACEE1920ESR- Embedded System and Real Time Programming VHDL Program using Xilinx

Assessment Questions with Answer

1. Which of the following is a primary characteristic of an embedded system?

- a) General-purpose functionality
- b) Real-time operation
- c) High power consumption
- d) Extensive user interface

Answer: b) Real-time operation

2. In VHDL, what does the acronym VHDL stand for?

- a) Variable High-Density Language
- b) Verilog Hardware Description Language
- c) Very High-Speed Integrated Circuit Hardware Description Language
- d) Visual Hardware Design Language

Answer: c) Very High-Speed Integrated Circuit Hardware Description Language

3. What is the purpose of the 'entity' declaration in VHDL?

- a) To define the internal architecture
- b) To specify the external interface
- c) To initiate signal processes
- d) To allocate memory

Answer: b) To specify the external interface

4. Which Xilinx software tool is primarily used for synthesizing VHDL code?

- a) ModelSim
- b) ISE (Integrated Software Environment)
- c) Quartus II
- d) Proteus

Answer: b) ISE (Integrated Software Environment)

5. What is the role of the 'architecture' declaration in VHDL?

- a) To specify the external interface
- b) To describe the internal behavior and structure

- c) To define the clock frequency
- d) To set up testbenches

Answer: b) To describe the internal behavior and structure

6. In VHDL, what is the function of a 'signal'?

- a) To declare variables for simulation
- b) To describe the entity interface
- c) To connect different parts of the design
- d) To store values temporarily

Answer: c) To connect different parts of the design

7. Which of the following is a common use of VHDL in embedded systems?

- a) Developing operating systems
- b) Designing hardware components
- c) Writing application software
- d) Implementing network protocols

Answer: b) Designing hardware components

8. What is the main advantage of using FPGAs in embedded systems?

- a) Lower power consumption compared to ASICs
- b) High flexibility and reconfigurability
- c) Simplified programming process
- d) Extensive built-in peripherals

Answer: b) High flexibility and reconfigurability

9. In a real-time system, what does the term "deadline" refer to?

- a) The time by which a task must start
- b) The maximum allowable response time
- c) The time by which a task must complete
- d) The duration a task can be delayed

Answer: c) The time by which a task must complete

10. What does the 'process' statement in VHDL define?

- a) A continuous concurrent operation
- b) A sequential block of code
- c) A variable declaration block
- d) An external interface specification

Answer: b) A sequential block of code



PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

(Approved by AICTE & Affiliated to Anna University, Chennai)

Madurai - Sivaganga Highway, Arasankoor, Theumansolai Post, Sivagangai Dt - 630 601, Tamilnadu
Mobile: 9842102628, 7373002628 Email: info@psyec.edu.in Website: www.psyec.edu.in

City Office: 10, Pandian Saraswathi St, Sivagami Nagar, Narayanasapuram, Madurai - 625 014. Telefax: 0452 2687338, Mobile: 98423 02628

Department of Electrical And Electronics Engineering

Academic Year 2019-2020

VACEE1920ESR- Embedded System and Real Time Programming VHDL Program

using Xilinx

Assessment Test Paper

REGISTER NUMBER: 912017105018

NAME OF THE STUDENT: SANTHOSH.

9/10

- Which of the following is a primary characteristic of an embedded system?
a) General-purpose functionality
b) Real-time operation
c) High power consumption
d) Extensive user interface
- In VHDL, what does the acronym VHDL stand for?
a) Variable High-Density Language
b) Verilog Hardware Description Language
c) Very High-Speed Integrated Circuit Hardware Description Language
d) Visual Hardware Design Language
- What is the purpose of the 'entity' declaration in VHDL?
a) To define the internal architecture
b) To specify the external interface
c) To initiate signal processes
d) To allocate memory
- Which Xilinx software tool is primarily used for synthesizing VHDL code?
a) ModelSim
b) ISE (Integrated Software Environment)
c) Quartus II
d) Proteus
- What is the rôle of the 'architecture' declaration in VHDL?
a) To specify the external interface
b) To describe the internal behavior and structure
c) To define the clock frequency
d) To set up testbenches
- In VHDL, what is the function of a 'signal'?
a) To declare variables for simulation
b) To describe the entity interface
c) To connect different parts of the design
d) To store values temporarily

Which of the following is a common use of VHDL in embedded systems?

- a) Developing operating systems
- b) Designing hardware components
- c) Writing application software
- d) Implementing network protocols



8. What is the main advantage of using FPGAs in embedded systems?

- a) Lower power consumption compared to ASICs
- b) High flexibility and reconfigurability
- c) Simplified programming process
- d) Extensive built-in peripherals



9. In a real-time system, what does the term "deadline" refer to?

- a) The time by which a task must start
- b) The maximum allowable response time
- c) The time by which a task must complete
- d) The duration a task can be delayed



10. What does the 'process' statement in VHDL define?

- a) A continuous concurrent operation
- b) A sequential block of code
- c) A variable declaration block
- d) An external interface specification



Pandian Saraswathi yadav Engineering College, Arasanoor -630561

Department of Electrical and Electronics Engineering

Student Performance Sheet

Academic Year : 2019-2020

Course Code : VACEE1920ESR

Course Name : ~~For~~ For Embedded System and Real Time Programming VHDL Program using Xilinx

Duration of hours : 35

Period of Course : 02.06.2020 to 06.06.2020

Assessment marks			Marks
Sl. No	Register Number	Student Name	
1	912017105002	M.ABARNA	95
2	912017105005	S.HARIBALAN	94
3	912017105006	T.JEYARAJ	93
4	912017105008	R.JOHN ROBERT	92
5	912017105009	R.JOYS PREETHI	91
6	912017105010	M.KARTHICK	74
7	912017105011	MOTHI BALA VISHAGAN	99
8	912017105013	M.NAVEEN PRASATH	100
9	912017105015	R.ROBIN	96
10	912017105016	B.P.SAKTHI	98
11	912017105017	P.SAKTHI VISHNU PRIYAN	99
12	912017105018	WASANTH SANTHOSH	90
13	912017105019	R.SUBA	91
14	912017105020	S.THIRUBAKARAN	92
15	912017105021	P.USHA NANDHINI	93
16	912017105022	R.VENKAT MURUGAN	94
17	912017105023	M.VINOTH KUMAR	95
18	912017105024	B.YASHIWANTH KUMAR	96
19	912017105303	S.SENTHILNATHAN	98
20	912016105001	AJITH KUMAR M	99
21	912016105002	ARUN KUMAR K	80
22	912016105003	DIVYA DHARSHINI K	83
23	912016105006	KRISHNA KUMAR M.	82
24	912016105008	MEETRA R	84
25	912016105011	RAGHURAMAN.V	85
26	912016105012	SEETHUPATHI D.	86
27	912016105013	SHALINI J	88
28	912016105014	SARANJEEVI	87
29	912016105017	TAMILSELVIM	70
30	912016105018	VASANTH M	71
31	912016105019	VARAJANGI	72
32	912016105302	VGNEESH P	73
33	912016105502	MAMBHARANIS	74

Tea Break

FN- 11:00 am to 11:15am & AN-03:00 pm to 03:15 pm

Lunch Break

12:15 pm to 01:00pm

Kalai Selvi
Course coordinator

PRINCIPAL



PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

(Approved by AICTE & Affiliated to Anna University, Chennai)

Madurai - Sivagangai Highway, Arasanoor, Thirumansolai Post, Sivagangai Dt. - 630 561, Tamilnadu
Mobile : 9842102628, 7373002628 Email: info@psyec.edu.in Website : www.psyec.edu.in

City Office : 10, Pandian Saraswathi St, Sivagami Nagar, Narayanapuram, Madurai - 625 014. Telefax- 0452 2682338, Mobile : 98423-02628

Department of Electrical And Electronics Engineering

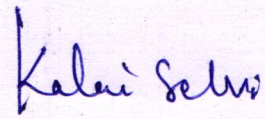
Academic Year 2019-2020

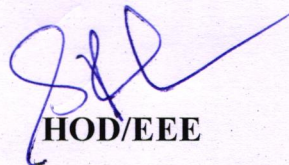
**VACEE1920ESR- Embedded System and Real Time Programming VHDL Program
using Xilinx**

ASSESSMENT MODE

In order to get a certificate for this course, the students should satisfy the following constraints

Attendance : 75 %
Assessment Question : MCQ pattern
Assessment Mark : Greater than or equal to 50%


Course Coordinator


HOD/EEE


PRINCIPAL

STUDENTS ATTENDANCE

Student Attendance Sheet

Academic Year : 2019-2020

Course Code : VACEE1920ESR

Course Name : Embedded System and Real Time Programming VHDL Program using Xilinx

Duration of hours : 35

Period of Course : 02.06.20-06.06.20

Attendance Sheet			Date: 2-6-20 - 6-6-20.					
Sl. No	Register Number	Student Name	09.00 am - 10.00 am	10.00 am - 11.00 am	11.15 am - 12.15pm	01.00 pm - 02.00 pm	02.00 pm - 03.00 pm	03.15 pm - 04.15 pm
1	912017105002	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA
2	912017105005	S.HARIBALAN	HARIBALAN	HARIBALAN	HARIBALAN	HARIBALAN	HARIBALAN	HARIBALAN
3	912017105006	T.JEYARAJ	T.JEYARAJ	T.JEYARAJ	T.JEYARAJ	T.JEYARAJ	T.JEYARAJ	T.JEYARAJ
4	912017105008	R.JOHN ROBERT	JOHN ROBERT	JOHN ROBERT	JOHN ROBERT	JOHN ROBERT	JOHN ROBERT	JOHN ROBERT
5	912017105009	R.JOYS PREETHI	R.JOYS PREETHI	R.JOYS PREETHI	R.JOYS PREETHI	R.JOYS PREETHI	R.JOYS PREETHI	R.JOYS PREETHI
6	912017105010	M.KARTHICK	KARTHICK	KARTHICK	KARTHICK	KARTHICK	KARTHICK	KARTHICK
7	912017105011	MOTHI BALA VISHAGAN	BALA VISHAGAN	BALA VISHAGAN	BALA VISHAGAN	BALA VISHAGAN	BALA VISHAGAN	BALA VISHAGAN
8	912017105013	M.NAVEEN PRASATH	NAVEEN PRASATH	NAVEEN PRASATH	NAVEEN PRASATH	NAVEEN PRASATH	NAVEEN PRASATH	NAVEEN PRASATH
9	912017105015	R.ROBIN	ROBIN	ROBIN	ROBIN	ROBIN	ROBIN	ROBIN
10	912017105016	B.P.SAKTHI	SAKTHI	SAKTHI	SAKTHI	SAKTHI	SAKTHI	SAKTHI
11	912017105017	P.SAKTHI VISHNU PRIYAN	VISHNU PRIYAN	VISHNU PRIYAN	VISHNU PRIYAN	VISHNU PRIYAN	VISHNU PRIYAN	VISHNU PRIYAN
12	912017105018	W.SANTHOSH	SANTHOSH	SANTHOSH	SANTHOSH	SANTHOSH	SANTHOSH	SANTHOSH
13	912017105019	R.SUBA	SUBA	SUBA	SUBA	SUBA	SUBA	SUBA
14	912017105020	S.THIRUBAKARAN	THIRUBAKARAN	THIRUBAKARAN	THIRUBAKARAN	THIRUBAKARAN	THIRUBAKARAN	THIRUBAKARAN
15	912017105021	P.USHA NANDHINI	USHA NANDHINI	USHA NANDHINI	USHA NANDHINI	USHA NANDHINI	USHA NANDHINI	USHA NANDHINI
16	912017105022	R.VENKAT MURUGAN	MURUGAN	MURUGAN	MURUGAN	MURUGAN	MURUGAN	MURUGAN
17	912017105023	M.VINOTH KUMAR	VINOTH KUMAR	VINOTH KUMAR	VINOTH KUMAR	VINOTH KUMAR	VINOTH KUMAR	VINOTH KUMAR
18	912017105024	B.YASHWANTH KUMAR	YASHWANTH KUMAR	YASHWANTH KUMAR	YASHWANTH KUMAR	YASHWANTH KUMAR	YASHWANTH KUMAR	YASHWANTH KUMAR
19	912017105303	S.SENTHILNATHAN	SENTHILNATHAN	SENTHILNATHAN	SENTHILNATHAN	SENTHILNATHAN	SENTHILNATHAN	SENTHILNATHAN
20	912016105001	AJITH KUMAR M	AJITH KUMAR M	AJITH KUMAR M	AJITH KUMAR M	AJITH KUMAR M	AJITH KUMAR M	AJITH KUMAR M
21	912016105002	ARUN KUMAR K	ARUN KUMAR K	ARUN KUMAR K	ARUN KUMAR K	ARUN KUMAR K	ARUN KUMAR K	ARUN KUMAR K
22	912016105003	DIVYA DHARSHINI K	DIVYA DHARSHINI K	DIVYA DHARSHINI K	DIVYA DHARSHINI K	DIVYA DHARSHINI K	DIVYA DHARSHINI K	DIVYA DHARSHINI K
23	912016105006	KRISHNAKUMAR M	KRISHNAKUMAR M	KRISHNAKUMAR M	KRISHNAKUMAR M	KRISHNAKUMAR M	KRISHNAKUMAR M	KRISHNAKUMAR M
24	912016105008	MITRA R	MITRA R	MITRA R	MITRA R	MITRA R	MITRA R	MITRA R
25	912016105011	RAGHOTHAMAN V	RAGHOTHAMAN V	RAGHOTHAMAN V	RAGHOTHAMAN V	RAGHOTHAMAN V	RAGHOTHAMAN V	RAGHOTHAMAN V
26	912016105012	SETHUPATHI D	SETHUPATHI D	SETHUPATHI D	SETHUPATHI D	SETHUPATHI D	SETHUPATHI D	SETHUPATHI D
27	912016105013	SHALINI J	SHALINI J	SHALINI J	SHALINI J	SHALINI J	SHALINI J	SHALINI J
28	912016105014	SIRANJEEVI R	SIRANJEEVI R	SIRANJEEVI R	SIRANJEEVI R	SIRANJEEVI R	SIRANJEEVI R	SIRANJEEVI R
29	912016105017	TAMILSELVI M	TAMILSELVI M	TAMILSELVI M	TAMILSELVI M	TAMILSELVI M	TAMILSELVI M	TAMILSELVI M
30	912016105018	VASANTH M	VASANTH M	VASANTH M	VASANTH M	VASANTH M	VASANTH M	VASANTH M
31	912016105019	YUVARAJAN G	YUVARAJAN G	YUVARAJAN G	YUVARAJAN G	YUVARAJAN G	YUVARAJAN G	YUVARAJAN G
32	912016105302	VIGNESH P	VIGNESH P	VIGNESH P	VIGNESH P	VIGNESH P	VIGNESH P	VIGNESH P
33	912016105502	MANIBHARATH S	MANIBHARATH S	MANIBHARATH S	MANIBHARATH S	MANIBHARATH S	MANIBHARATH S	MANIBHARATH S

Kalai Selvi
Course coordinator

[Signature]
HOD/EEE

[Signature]
PRINCIPAL

Student Attendance Sheet

Academic Year : 2019-2020

Course Code : VACEE1920ESR

Course Name : Embedded System and Real Time Programming VHDL Program using Xilinx

Duration of hours : 35

Period of Course : 02.06.20-06.06.20

Attendance Sheet			Date: 2.6.20 - 6.6.20					
Sl. No	Register Number	Student Name	09.00 am - 10.00 am	10.00 am - 11.00 am	11.15 am - 12.15pm	01.00 pm - 02.00 pm	02.00 pm - 03.00 pm	03.15 pm - 04.15 pm
1	912017105002	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA
2	912017105005	S.HARIBALAN	Hariba	Haribal	Hariba	Haribal	Haribal	Haribal
3	912017105006	T.JEYARAJ	T.Jey	T.Jey	T.Jey	T.Jey	T.Jey	T.Jey
4	912017105008	R.JOHN ROBERT	John	John	John	John	John	John
5	912017105009	R.JOYS PREETHI	Joy	Joy	Joy	Joy	Joy	Joy
6	912017105010	M.KARTHICK	Karth	Karth	Karth	Karth	Karth	Karth
7	912017105011	MOTHI BALA VISHAGAN	Bala	Bala	Bala	Bala	Bala	Bala
8	912017105013	M.NAVEEN PRASATH	Naveen	Naveen	Naveen	Naveen	Naveen	Naveen
9	912017105015	R.ROBIN	Robi	Robi	Robi	Robi	Robi	Robi
10	912017105016	B.P.SAKTHI	Sakthi	Sakthi	Sakthi	Sakthi	Sakthi	Sakthi
11	912017105017	P.SAKTHI VISHNU PRIYAN	Sakthi	Vishnu	Vishnu	Vishnu	Vishnu	Vishnu
12	912017105018	W.SANTHOSH	Santhosh	Santhosh	Santhosh	Santhosh	Santhosh	Santhosh
13	912017105019	R.SUBA	Suba	Suba	Suba	Suba	Suba	Suba
14	912017105020	S.THIRUBAKARAN	Thiru	Thiru	Thiru	Thiru	Thiru	Thiru
15	912017105021	P.USHA NANDHINI	Usha	Usha	Usha	Usha	Usha	Usha
16	912017105022	R.VENKAT MURUGAN	Murugan	Murugan	Murugan	Murugan	Murugan	Murugan
17	912017105023	M.VINOTH KUMAR	Vinodh	Vinodh	Vinodh	Vinodh	Vinodh	Vinodh
18	912017105024	B.YASHWANTH KUMAR	Yash	Yash	Yash	Yash	Yash	Yash
19	912017105303	S.SENTHILNATHAN	Senthil	Senthil	Senthil	Senthil	Senthil	Senthil
20	912016105001	AJITH KUMAR M	Ajith	Ajith	Ajith	Ajith	Ajith	Ajith
21	912016105002	ARUN KUMAR K	Arun	Arun	Arun	Arun	Arun	Arun
22	912016105003	DIVYA DHARSHINI K	Divya	Divya	Divya	Divya	Divya	Divya
23	912016105006	KRISHNAKUMAR M	MKD	MKD	MKD	MKD	MKD	MKD
24	912016105008	MITRA R	Mitra	Mitra	Mitra	Mit	Mit	Mit
25	912016105011	RAGHOTHAMAN V	RKD	RKD	RKD	RKD	RKD	RKD
26	912016105012	SETHUPATHI D	Sethu	Sethu	Sethu	Sethu	Sethu	Sethu
27	912016105013	SHALINI J	J.S	J.S	J.S	J.S	J.S	J.S
28	912016105014	SIRANJEEVI R	R.Sir	R.Sir	R.Sir	R.Sir	R.Sir	R.Sir
29	912016105017	TAMILSELVI M	M.T	M.T	M.T	M.T	M.T	M.T
30	912016105018	VASANTH M	M.V	M.V	M.V	M.V	M.V	M.V
31	912016105019	YUVARAJAN G	G.Y	G.Y	G.Y	G.Y	G.Y	G.Y
32	912016105302	VIGNESH P	P.V	P.V	P.V	P.V	P.V	P.V
33	912016105502	MANIBHARATH S	M.S	M.S	M.S	M.S	M.S	M.S

Kalai Selvi
Course coordinator


WOD/EEE


PRINCIPAL

Student Attendance Sheet

Academic Year : 2019-2020

Course Code : VACEE1920ESR

Course Name : Embedded System and Real Time Programming VHDL Program using Xilinx

Duration of hours : 35

Period of Course : 02.06.20-06.06.20

Attendance Sheet			Date: 2.6.20 - 6.6.20.					
Sl. No	Register Number	Student Name	09.00 am - 10.00 am	10.00 am - 11.00 am	11.15 am - 12.15pm	01.00 pm - 02.00 pm	02.00 pm - 03.00 pm	03.15 pm - 04.15 pm
1	912017105002	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA	M.ABARNA
2	912017105005	S.HARIBALAN	S.HARIBALAN	S.HARIBALAN	S.HARIBALAN	S.HARIBALAN	S.HARIBALAN	S.HARIBALAN
3	912017105006	T.JEYARAJ	Jeyaraj	Jeyaraj	Jeyaraj	Jeyaraj	Jeyaraj	Jeyaraj
4	912017105008	R.JOHN ROBERT	RJO	RJO	RJO	RJO	RJO	RJO
5	912017105009	R.JOYS PREETHI	Joy	Joy	Joy	Joy	Joy	Joy
6	912017105010	M.KARTHICK	Kirk	Kirk	Kirk	Kirk	Kirk	Kirk
7	912017105011	MOTHI BALA VISHAGAN	M.BV	M.BV	M.BV	M.BV	M.BV	M.BV
8	912017105013	M.NAVEEN PRASATH	M.NAVEEN	M.NAVEEN	M.NAVEEN	M.NAVEEN	M.NAVEEN	M.NAVEEN
9	912017105015	R.ROBIN	ROBIN	ROBIN	ROBIN	ROBIN	ROBIN	ROBIN
10	912017105016	B.P.SAKTHI	B.P	B.P	B.P	B.P	B.P	B.P
11	912017105017	P.SAKTHI VISHNU PRIYAN	P.SV	P.SV	P.SV	P.SV	P.SV	P.SV
12	912017105018	W.SANTHOSH	W.S	W.S	W.S	W.S	W.S	W.S
13	912017105019	R.SUBA	Suba	Suba	Suba	Suba	Suba	Suba
14	912017105020	S.THIRUBAKARAN	ST	ST	ST	ST	ST	ST
15	912017105021	P.USHA NANDHINI	P.U	P.U	P.U	P.U	P.U	P.U
16	912017105022	R.VENKAT MURUGAN	R.VM	R.VM	R.VM	R.VM	R.VM	R.VM
17	912017105023	M.VINOTH KUMAR	Vinoth	Vinoth	Vinoth	Vinoth	Vinoth	Vinoth
18	912017105024	B.YASHWANTH KUMAR	B.Y	B.Y	B.Y	B.Y	B.Y	B.Y
19	912017105303	S.SENTHILNATHAN	S.S	S.S	S.S	S.S	S.S	S.S
20	912016105001	AJITH KUMAR M	Ajith	Ajith	Ajith	Ajith	Ajith	Ajith
21	912016105002	ARUN KUMAR K	Arun	Arun	Arun	Arun	Arun	Arun
22	912016105003	DIVYA DHARSHINI K	Divya	Divya	Divya	Divya	Divya	Divya
23	912016105006	KRISHNAKUMAR M	M.K	M.K	M.K	M.K	M.K	M.K
24	912016105008	MITRA R	R.MITRA	R.MITRA	R.MITRA	R.MITRA	R.MITRA	R.MITRA
25	912016105011	RAGHOTHAMAN V	R.V	R.V	R.V	R.V	R.V	R.V
26	912016105012	SETHUPATHI D	D.S	D.S	D.S	D.S	D.S	D.S
27	912016105013	SHALINI J	J.S	J.S	J.S	J.S	J.S	J.S
28	912016105014	SIRANJEEVI R	R.S	R.S	R.S	R.S	R.S	R.S
29	912016105017	TAMILSELVI M	M.T	M.T	M.T	M.T	M.T	M.T
30	912016105018	VASANTH M	M.V	M.V	M.V	M.V	M.V	M.V
31	912016105019	YUVARAJAN G	G.Y	G.Y	G.Y	G.Y	G.Y	G.Y
32	912016105302	VIGNESH P	P.V	P.V	P.V	P.V	P.V	P.V
33	912016105502	MANIBHARATH S	S.M	S.M	S.M	S.M	S.M	S.M

Kalai Selvi

Course coordinator

[Signature]

HOD/EEE

[Signature]

PRINCIPAL

Student Attendance Sheet

Academic Year : 2019-2020

Course Code : VACEE1920ESR

Course Name : Embedded System and Real Time Programming VHDL Program using Xilinx

Duration of hours : 35

Period of Course : 02.06.20-06.06.20

Attendance Sheet			Date: 2.6.20 - 6.6.20					
Sl. No	Register Number	Student Name	09.00 am - 10.00 am	10.00 am - 11.00 am	11.15 am - 12.15pm	01.00 pm - 02.00 pm	02.00 pm - 03.00 pm	03.15 pm - 04.15 pm
1	912017105002	M.ABARNA	M.Abarna	M.Abarna	M.Abarna	M.Abarna	M.Abarna	M.Abarna
2	912017105005	S.HARIBALAN	S.haribalan	S.haribalan	S.haribalan	S.haribalan	S.haribalan	S.haribalan
3	912017105006	T.JEYARAJ	Jeyaraj	Jeyaraj	Jeyaraj	Jeyaraj	Jeyaraj	Jeyaraj
4	912017105008	R.JOHN ROBERT	R.JO	R.JO	R.JO	R.JO	R.JO	R.JO
5	912017105009	R.JOYS PREETHI	Joy	Joy	Joy	Joy	Joy	Joy
6	912017105010	M.KARTHICK	Karthick	Karthick	Karthick	Karthick	Karthick	Karthick
7	912017105011	MOTHI BALA VISHAGAN	M.Balu	M.Balu	M.Balu	M.Balu	M.Balu	M.Balu
8	912017105013	M.NAVEEN PRASATH	M.naveen	M.naveen	M.naveen	M.naveen	M.naveen	M.naveen
9	912017105015	R.ROBIN	R.Robin	R.Robin	R.Robin	R.Robin	R.Robin	R.Robin
10	912017105016	B.P.SAKTHI	B.P	B.P	B.P	B.P	B.P	B.P
11	912017105017	P.SAKTHI VISHNU PRIYAN	P.S	P.S	P.S	P.S	P.S	P.S
12	912017105018	W.SANTHOSH	W.Su	W.Su	W.Su	W.Su	W.Su	W.Su
13	912017105019	R.SUBA	R.Suba	R.Suba	R.Suba	R.Suba	R.Suba	R.Suba
14	912017105020	S.THIRUBAKARAN	S.T	S.T	S.T	S.T	S.T	S.T
15	912017105021	P.USHA NANDHINI	P.U	P.U	P.U	P.U	P.U	P.U
16	912017105022	R.VENKAT MURUGAN	R.V	R.V	R.V	R.V	R.V	R.V
17	912017105023	M.VINOTH KUMAR	Vinoth	Vinoth	Vinoth	Vinoth	Vinoth	Vinoth
18	912017105024	B.YASHWANTH KUMAR	B.Y	B.Y	B.Y	B.Y	B.Y	B.Y
19	912017105303	S.SENTHILNATHAN	S.S	S.S	S.S	S.S	S.S	S.S
20	912016105001	AJITH KUMAR M	M.Ajith	M.Ajith	M.Ajith	M.Ajith	M.Ajith	M.Ajith
21	912016105002	ARUN KUMAR K	Arun	Arun	Arun	Arun	Arun	Arun
22	912016105003	DIVYA DHARSHINI K	Divya	Divya	Divya	Divya	Divya	Divya
23	912016105006	KRISHNAKUMAR M	M.K	M.K	M.K	M.K	M.K	M.K
24	912016105008	MITRA R	R.MITRA	R.MITRA	R.MITRA	R.MITRA	R.MITRA	R.MITRA
25	912016105011	RAGHOTHAMAN V	R.V	R.V	R.V	R.V	R.V	R.V
26	912016105012	SETHUPATHI D	D.S	D.S	D.S	D.S	D.S	D.S
27	912016105013	SHALINI J	J.S	J.S	J.S	J.S	J.S	J.S
28	912016105014	SIRANJEEVI R	R.Sir	R.Sir	R.Sir	R.Sir	R.Sir	R.Sir
29	912016105017	TAMILSELVI M	M.T	M.T	M.T	M.T	M.T	M.T
30	912016105018	VASANTH M	M.V	M.V	M.V	M.V	M.V	M.V
31	912016105019	YUVARAJAN G	G.Y	G.Y	G.Y	G.Y	G.Y	G.Y
32	912016105302	VIGNESH P	P.Vign	P.Vign	P.Vign	P.Vign	P.Vign	P.Vign
33	912016105502	MANIBHARATH S	S.M	S.M	S.M	S.M	S.M	S.M

Kalai Selvi
Course coordinator

[Signature]
HOD/EEE

[Signature]
PRINCIPAL

Academic Year : 2019-2020

Course Code : VACEE1920ESR

Course Name : Embedded System and Real Time Programming VHDL Program using Xilinx

Duration of hours : 35

Period of Course : 02.06.20-06.06.20

Attendance Sheet			Date: 2.6.20 - 6.6.20					
Sl. No	Register Number	Student Name	09.00 am - 10.00 am	10.00 am - 11.00 am	11.15 am - 12.15pm	01.00 pm - 02.00 pm	02.00 pm - 03.00 pm	03.15 pm - 04.15 pm
1	912017105002	M.ABARNA	M.Abar	M.Abar	M.Abar	M.Abar	M.Abar	M.Abar
2	912017105005	S.HARIBALAN	S.haribala	S.haribala	S.haribala	S.haribala	S.haribala	S.haribala
3	912017105006	T.JEYARAJ	Jeyaraj	Jeyaraj	Jeyaraj	Jeyaraj	Jeyaraj	Jeyaraj
4	912017105008	R.JOHN ROBERT	JOHN	JOHN	JOHN	JOHN	JOHN	JOHN
5	912017105009	R.JOYS PREETHI	R.P.P	R.P.P	R.P.P	R.P.P	R.P.P	R.P.P
6	912017105010	M.KARTHICK	Kanck	Kanck	Kanck	Kanck	Kanck	Kanck
7	912017105011	MOTHI BALA VISHAGAN	M.B.V	M.B.V	M.B.V	M.B.V	M.B.V	M.B.V
8	912017105013	M.NAVEEN PRASATH	M.naveen	M.naveen	M.naveen	M.naveen	M.naveen	M.naveen
9	912017105015	R.ROBIN	R.Robin	R.Robin	R.Robin	R.Robin	R.Robin	R.Robin
10	912017105016	B.P.SAKTHI	B.P	B.P	B.P	B.P	B.P	B.P
11	912017105017	P.SAKTHI VISHNU PRIYAN	P.S.V	P.S.V	P.S.V	P.S.V	P.S.V	P.S.V
12	912017105018	W.SANTHOSH	W.Sun	W.Sun	W.Sun	W.Sun	W.Sun	W.Sun
13	912017105019	R.SUBA	R.Suba	R.Suba	R.Suba	R.Suba	R.Suba	R.Suba
14	912017105020	S.THIRUBAKARAN	S.T	S.T	S.T	S.T	S.T	S.T
15	912017105021	P.USHA NANDHINI	P.U	P.U	P.U	P.U	P.U	P.U
16	912017105022	R.VENKAT MURUGAN	R.V	R.V	R.V	R.V	R.V	R.V
17	912017105023	M.VINOTH KUMAR	vinoth	vinoth	vinoth	vinoth	vinoth	vinoth
18	912017105024	B.YASHWANTH KUMAR	B.Y	B.Y	B.Y	B.Y	B.Y	B.Y
19	912017105303	S.SENTHILNATHAN	S.S	S.S	S.S	S.S	S.S	S.S
20	912016105001	AJITH KUMAR M	M.Ajith	M.Ajith	M.Ajith	M.Ajith	M.Ajith	M.Ajith
21	912016105002	ARUN KUMAR K	Arun	Arun	Arun	Arun	Arun	Arun
22	912016105003	DIVYA DHARSHINI K	Divya	Divya	Divya	Divya	Divya	Divya
23	912016105006	KRISHNAKUMAR M	M.K	M.K	M.K	M.K	M.K	M.K
24	912016105008	MITRA R	R.MITRA	R.MITRA	R.MITRA	R.MITRA	R.MITRA	R.MITRA
25	912016105011	RAGHOTHAMAN V	R.V	R.V	R.V	R.V	R.V	R.V
26	912016105012	SETHUPATHI D	D.S	D.S	D.S	D.S	D.S	D.S
27	912016105013	SHALINI J	J.S	J.S	J.S	J.S	J.S	J.S
28	912016105014	SIRANJEEVI R	R.Sir	R.Sir	R.Sir	R.Sir	R.Sir	R.Sir
29	912016105017	TAMILSELVI M	M.T	M.T	M.T	M.T	M.T	M.T
30	912016105018	VASANTH M	M.V	M.V	M.V	M.V	M.V	M.V
31	912016105019	YUVARAJAN G	G.Yu	G.Yu	G.Yu	G.Yu	G.Yu	G.Yu
32	912016105302	VIGNESH P	P.Vign	P.Vign	P.Vign	P.Vign	P.Vign	P.Vign
33	912016105502	MANIBHARATH S	S.M	S.M	S.M	S.M	S.M	S.M

Kalai Selvi
Course coordinator

[Signature]
HOD/EEE

[Signature]
PRINCIPAL

Enrollment
Student Name
List

Pandian Saraswathi yadav Engineering College, Arasanoor -630561

Department of Electrical And Electronics Engineering

Student Registration Sheet

Academic Year : 2019-2020

Course Code : VACEE1920ESR

Course Name : Embedded System and Real Time Programming VHDL Program using Xilinx

Duration of hours : 35

Period of Course : 02.06.20-06.06.20

Enrolled Students List			Signature
Sl. No	Register Number	Student Name	
1	912017105002	M.ABARNA	M. ABARNA
2	912017105005	S.HARIBALAN	Haru
3	912017105006	T.JEYARAJ	TJEY
4	912017105008	R.JOHN ROBERT	John
5	912017105009	R.JOYS PREETHI	R. JOY
6	912017105010	M.KARTHICK	Karthick
7	912017105011	MOTHI BALA VISHAGAN	Bala
8	912017105013	M.NAVEEN PRASATH	Naveen
9	912017105015	R.ROBIN	Robin
10	912017105016	B.P.SAKTHI	Sakthi
11	912017105017	P.SAKTHI VISHNU PRIYAN	Vishi
12	912017105018	W.SANTHOSH	Santhosh
13	912017105019	R.SUBA	Suba
14	912017105020	S.THIRUBAKARAN	Thiru
15	912017105021	P.USHA NANDHINI	Usha
16	912017105022	R.VENKAT MURUGAN	Venkat
17	912017105023	M.VINOTH KUMAR	Vinath
18	912017105024	B.YASHWANTH KUMAR	Yash
19	912017105303	S.SENTHILNATHAN	Senthil
20	912016105001	AJITH KUMAR M	Ajith
21	912016105002	ARUN KUMAR K	Arun
22	912016105003	DIVYA DHARSHINI K	Divya
23	912016105006	KRISHNAKUMAR M	Krishna
24	912016105008	MITRA R	Mittra R
25	912016105011	RAGHOTHAMAN V	Raghu
26	912016105012	SETHUPATHI D	Sethu
27	912016105013	SHALINI J	Shalini
28	912016105014	SIRANJEEVI R	Siranjeevi
29	912016105017	TAMILSELVI M	Tamil
30	912016105018	VASANTH M	Vasanti
31	912016105019	YUVARAJAN G	Yuv
32	912016105302	VIGNESH P	Vignesh P
33	912016105502	MANIBHARATH S	Man

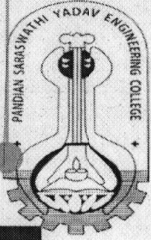
Tea Break FN- 11:00 am to 11:15am & AN-03:00 pm to 03:15 pm

Lunch Break 12:15 pm to 01:00pm

Kalai Selvi
Course coordinator HOB/EEE

PRINCIPAL

MODEL
CERTIFICATES



PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

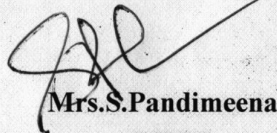
Approved by AICTE & Affiliated to Anna University, Chennai.
Arasanoor, Thirumansolai Post, Sivagangai – Madurai Highway, Tamilnadu - 630 561

Value added course on Embedded System And Real Time Programming VHDL Program Using XILINUX


Organized by
DEPARTMENT OF ELECTRICAL AND ELECTRONICS
ENGINEERING

CERTIFICATE

This is Certify that R. ROBIN From **Third and Final year EEE** has participated in the value-added course on Embedded System And Real Time Programming VHDL Program Using XILINUX organized by the Department of Electrical And Electronics Engineering From 02.06.2020 to 06.06.2020 (35 Hours) at Pandian Saraswathi Yadav Engineering College, Sivagangai.

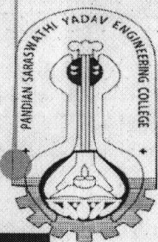

Mrs.S.Pandimeena
AP/EEE

Head of the Department


Dr.R.RAJA
Principal

R
RAJA

Digitally signed
by R RAJA
Date: 2024.07.15
15:19:20 +05'30'



PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

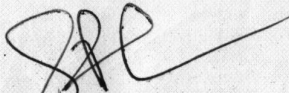
Approved by AICTE & Affiliated to Anna University, Chennai.
Arasanoor, Thirumansolai Post, Sivagangai – Madurai Highway, Tamilnadu - 630 561

Value added course on Embedded System And Real Time Programming VHDL Program Using XILINUX

Organized by
DEPARTMENT OF ELECTRICAL AND ELECTRONICS
ENGINEERING

CERTIFICATE

This is Certify that**M.KARTHICK**..... From **Third and Final year EEE** has participated in the value-added course on Embedded System And Real Time Programming VHDL Program Using XILINUX organized by the Department of Electrical And Electronics Engineering From 02.06.2020 to 06.06.2020 (35 Hours) at Pandian Saraswathi Yadav Engineering College, Sivagangai.

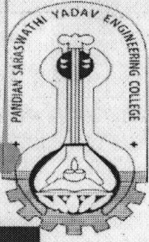

Mrs. S. Pandimeena
AP/EEE

Head of the Department


Dr. R. RAJA
Principal

R
RAJA

Digitally signed
by R RAJA
Date:
2024.07.15
15:19:38 +05'30'



PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE


Approved by AICTE & Affiliated to Anna University, Chennai.
Arasanoor, Thirumansolai Post, Sivagangai – Madurai Highway, Tamilnadu - 630 561

Value added course on Embedded System And Real Time Programming VHDL Program Using XILINUX


Organized by
DEPARTMENT OF ELECTRICAL AND ELECTRONICS
ENGINEERING

CERTIFICATE

This is Certify that DIVYA DHARSHINI K. From **Third and Final year EEE** has participated in the value-added course on Embedded System And Real Time Programming VHDL Program Using XILINUX organized by the Department of Electrical And Electronics Engineering From 02.06.2020 to 06.06.2020 (35 Hours) at Pandian Saraswathi Yadav Engineering College, Sivagangai.


Mrs.S.Pandimeena
AP/EEE

Head of the Department


Dr.R.RAJA
Principal

R
RAJA

Digitally signed by R RAJA
Date: 2024.07.15 15:19:58
+05'30'