# SYLLABUS/ CURRICULUM

# PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

(Approved by AICTE & Affiliated to Anna University, Chennai)

Madurai - Sivagangai Highway, Arasanoor, Thirumansolai Post, Sivagangai Dt. - 630 561, Tamilnadu
Mobile : 9842102628, 7373002628 Email: info@psyec.edu.in Website : www.psyec.edu.in

City Office : 10, Pandian Saraswathi St, Sivagami Nagar, Narayanapuram, Madurai - 625 014. Telefax- 0452 2682338, Mobile : 98423-02628


## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## COURSE SYLLABUS

## ACADEMIC YEAR 2021-2022

**' VACECE2122VLSI- VLSI Design using CADENCE Tools'**

**CHAPTER-1 Introduction to VLSI Design** 7

Overview of VLSI design flow-Introduction to Cadence design tools-Cadence Virtuoso Environment-Schematic capture using Virtuoso Schematic Editor (VSE)-Design rule checking (DRC) and layout versus schematic (LVS) verification-Digital Circuit Design

**CHAPTER-2 Combinational and sequential logic design** 7

Verilog-A and Verilog-AMS for digital modelling-Simulation using Cadence Incisive Analog Circuit Design

**CHAPTER-3 Basic analog building blocks** 7

Analog behavioral modeling (ABM) with Verilog-AMS-Analog simulation techniques-Layout Design-Principles of layout design-Floor planning and placement-Routing-techniques-Mixed-Signal Circuit Design

**CHAPTER-4 Integrating digital and analog components** 7

Mixed-signal simulation and verification-Design for Testability (DFT)- Built-in self-test (BIST) techniques-Scan chain insertion-Hands-On Projects:

**CHAPTER-5 Design and simulate a digital logic circuit using Cadence tools** 7

Design and simulate an analog amplifier circuit-Perform layout design and verification for a simple VLSI circuit-Integrate digital and analog components in a mixed-signal design

**TOTAL: 35Hrs**

M.Dhivya
COURSE COORDINATOR

R Raja
HOD/ECE

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PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE
Arasanoor, Thirumansolai P.O-630 561
Sivagangai Dt. Tamilnadu

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# PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## COURSE SCHEDULE

**VACECE2122VLSI- VLSI Design using CADENCE Tools**

| DATE | TIME | SYLLABUS |
|---|---|---|
| 04.04.2022 | 9.00AM TO 1.00PM<br>2.00PM TO 5.00PM | Overview of VLSI design flow-Introduction to Cadence design tools-Cadence Virtuoso Environment-Schematic capture using Virtuoso Schematic Editor (VSE)-Design rule checking (DRC) and layout versus schematic (LVS) verification-Digital Circuit Design |
| 05.04.2022 | 9.00AM TO 1.00PM<br>2.00PM TO 5.00PM | Verilog-A and Verilog-AMS for digital modelling-Simulation using Cadence Incisive Analog Circuit Design |
| 0604.2022 | 9.00AM TO 1.00PM<br>2.00PM TO 5.00PM | Analog behavioral modeling (ABM) with Verilog-AMS-Analog simulation techniques-Layout Design-Principles of layout design-Floor planning and placement-Routing-techniques-Mixed-Signal Circuit Design |
| 07.04.2022 | 9.00AM TO 1.00PM<br>2.00PM TO 5.00PM | Mixed-signal simulation and verification-Design for Testability (DFT)- Built-in self-test (BIST) techniques-Scan chain insertion-Hands-On Projects: |
| 08.04.2022 | 9.00AM TO 1.00PM<br>2.00PM TO 5.00PM<br>2.00PM TO 5.00PM | Design and simulate an analog amplifier circuit-Perform layout design and verification for a simple VLSI circuit-Integrate digital and analog components in a mixed-signal design |

Tea Break: 10:40 am to 10:55am & 02:45 pm to 15:00 pm

Lunch Break: 12:30pm to 01:00pm

TOTAL: 35hrs

COURSE COORDINATOR HOD / ECE PRINCIPAL

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ENGINEERING COLLEGE
Arasanoor, Thirumansolai P.O-630 561
Sivagangai Dist. Tamilnadu

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# PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**Academic Year 2022– 2023**

**One page Report**

| | |
|---|---|
| **Name of the course** | **: VLSI Design using CADENCE Tools** |
| **Course Code** | **: VACECE2122VLSI** |
| **Resource Person** | **: Dr.R.RAJA,ASP/ECE ,PSYEC** |
| **Course Coordinator** | **: Ms.M.DHIVYA BHARATHI,AP/ECE** |
| **Date/Duration** | : 04.04.2022-08.04.2022—35 hours |

I here affirm that the Final-year students of strength 32 have been taught the value-added course tittle "**VLSI Design using CADENCE Tools**" as per the syllabus and completed within the stipulated time duration.

I confirm that the value-added course titled "**VLSI Design using CADENCE Tools**" has been conducted in the beginning of the semester and course delivery along with the attendance of the students was recorded.

I confirmed that all the students were actively participated in the course and the eligible students were certified for the course.

M.Dhivya
**COURSE COORDINATOR**

R Raja
**HOD/ECE**

**PRINCIPAL**

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ENGINEERING COLLEGE
Arasanoor, Thirumansolai P.O-630 561
Sivagangai Dist. Tamilnadu

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# ASSESSMENT PROCEDURE

# PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## ASSESSMENT QUESTION WITH ANSWER

### VACECE2122VLSI- VLSI Design using CADENCE Tools

**1. What does VLSI stand for?**

a) Very Large Scale Integration

b) Very Long Semiconductor Integration

c) Virtual Logic System Integration

d) Variable Level Signal Integration

**Answer: a) Very Large Scale Integration**

**2. Which Cadence tool is commonly used for layout design?**

a) Virtuoso Layout Editor (VLE)

b) Virtuoso Schematic Editor (VSE)

c) Cadence Encounter

d) Cadence Incisive

**Answer: a) Virtuoso Layout Editor (VLE)**

**3. Which language is commonly used for digital modeling in Cadence tools?**

a) VHDL

b) Verilog

c) C++

d) Python

**Answer: b) Verilog**

**4. What does DRC stand for in the context of layout design?**

a) Design Review Checklist

b) Design Rule Checking

c) Device Routing Criteria

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d) Digital Routing Configuration

**Answer: b) Design Rule Checking**

**5. Which Cadence tool is used for digital simulation?**

a) Virtuoso Layout Editor (VLE)

b) Virtuoso Schematic Editor (VSE)

c) Cadence Incisive

d) Cadence Encounter

**Answer: c) Cadence Incisive**

**6. What is ABM in the context of analog circuit design?**

a) Analog Behavioral Modeling

b) Analog Bit Manipulation

c) Advanced Board Management

d) Automatic Biasing Mechanism

**Answer: a) Analog Behavioral Modeling**

**7. What is the purpose of floorplanning in layout design?**

a) To create a rough sketch of the layout

b) To plan the placement of components in the layout

c) To perform design rule checking

d) To simulate the circuit behavior

**Answer: b) To plan the placement of components in the layout**

**8. What does DFT stand for in the context of VLSI design?**

a) Digital Filter Technique

b) Design for Testability

c) Dynamic Fault Tolerance

d) Data Flow Testing

**Answer: b) Design for Testability**

**9. Which type of circuit design integrates both digital and analog components?**

a) Mixed-Signal Circuit Design

b) Hybrid Circuit Design

c) Integrated Circuit Design

d) Complex Circuit Design

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**Answer: a) Mixed-Signal Circuit Design**

**10. Which aspect of VLSI design focuses on ensuring that the fabricated chips are free from defects?**

a) Layout Optimization

b) Design for Manufacturability (DFM)

c) Static Timing Analysis (STA)

d) Power Analysis

**Answer: b) Design for Manufacturability (DFM)**

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## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### ASSESSMENT TEST PAPER

**VACECE2122VLSI- VLSI Design using CADENCE Tools**

REGISTER NO: 912020106001

NAME OF THE STUDENT: Ajaykannan

YEAR/SEM: II / IV

9/10

**1. What does VLSI stand for?**

a) Very Large Scale Integration

b) Very Long Semiconductor Integration

c) Virtual Logic System Integration

d) Variable Level Signal Integration

**2. Which Cadence tool is commonly used for layout design?**

a) Virtuoso Layout Editor (VLE)

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d) Cadence Incisive

**3. Which language is commonly used for digital modeling in Cadence tools?**

a) VHDL

b) Verilog

c) C++

d) Python

**4. What does DRC stand for in the context of layout design?**

a) Design Review Checklist

b) Design Rule Checking

c) Device Routing Criteria

d) Digital Routing Configuration

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**5. Which Cadence tool is used for digital simulation?**

a) Virtuoso Layout Editor (VLE)

b) Virtuoso Schematic Editor (VSE)

c) Cadence Incisive

d) Cadence Encounter

**6. What is ABM in the context of analog circuit design?**

a) Analog Behavioral Modeling

b) Analog Bit Manipulation

c) Advanced Board Management

d) Automatic Biasing Mechanism

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b) Hybrid Circuit Design

c) Integrated Circuit Design

d) Complex Circuit Design

**10. Which aspect of VLSI design focuses on ensuring that the fabricated chips are free from defects?**

a) Layout Optimization

b) Design for Manufacturability (DFM)

c) Static Timing Analysis (STA)

d) Power Analysis

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Pandian Saraswathi yadav Engineering College,Arasanoor -630561

Department of Electronics and Communication Engineering

Student Performance Sheet

Academic Year : 2021-2022

Cource Code : VACECE2122VLSI

Course Name : VLSI Design using CADENCE Tools

Duration of hours : 35

Period of Course : 04.04.2022-08.04.2022

| Assessment Mark | | | Mark |
|---|---|---|---|
| Sl. No | Register Number | Student Name | |
| 1 | 912020106001 | AJAYKANNAN M | 84 |
| 2 | 912020106002 | ANITHA S | 90 |
| 3 | 912020106003 | ANTONY BRIGHTON N | 98 |
| 4 | 912020106004 | BHAVANI SRI G | 93 |
| 5 | 912020106006 | GOKULASUTHAN M | 84 |
| 6 | 912020106007 | GOWSALYA K | 89 |
| 7 | 912020106008 | KABILAN M | 78 |
| 8 | 912020106009 | KANIMOZHI D | 98 |
| 9 | 912020106010 | KARTHIKA V | 89 |
| 10 | 912020106011 | NANTHA KUMAR V | 84 |
| 11 | 912020106012 | NIVETHA T | 89 |
| 12 | 912020106013 | PREETHI VAASHINI M | 99 |
| 13 | 912020106014 | RANJITH P | 79 |
| 14 | 912020106015 | SARAN VP | 68 |
| 15 | 912020106016 | SARAVANAN K | 70 |
| 16 | 912020106017 | SATHISHKUMAR M | 72 |
| 17 | 912020106018 | SIVANI S | 84 |
| 18 | 912020106019 | SUJITHA B | 89 |
| 19 | 912020106020 | THILOTHAMA M | 96 |
| 20 | 912020106021 | VALARMATHI S | 99 |
| 21 | 912020106301 | ARUMUGAM | 80 |
| 22 | 912020106302 | HARIVISHNU K | 80 |

Course coordinator

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# Enrollment Student Name List

Pandian Saraswathi yadav Engineering College,Arasanoor -630561

Department of Electronics and Communication Engineering

Student Registration Sheet

Academic Year : 2021-2022

Cource Code : VACECE2122VLSI

Course Name : VLSI Design using CADENCE Tools

Duration of hours : 35

Period of Course : 04.04.2022-08.04.2022

| Enrolled student list | | | Signature |
|---|---|---|---|
| Sl. No | Register Number | Student Name | |
| 1 | 912020106001 | AJAYKANNAN M | |
| 2 | 912020106002 | ANITHA S | Anitha.S |
| 3 | 912020106003 | ANTONY BRIGHTON N | |
| 4 | 912020106004 | BHAVANI SRI G | |
| 5 | 912020106006 | GOKULASUTHAN M | G.M |
| 6 | 912020106007 | GOWSALYA K | |
| 7 | 912020106008 | KABILAN M | Kabilan |
| 8 | 912020106009 | KANIMOZHI D | D. Kani |
| 9 | 912020106010 | KARTHIKA V | |
| 10 | 912020106011 | NANTHA KUMAR V | |
| 11 | 912020106012 | NIVETHA T | Nivetha |
| 12 | 912020106013 | PREETHI VAASHINI M | Preethi |
| 13 | 912020106014 | RANJITH P | |
| 14 | 912020106015 | SARAN VP | Saran VP |
| 15 | 912020106016 | SARAVANAN K | Saravanan |
| 16 | 912020106017 | SATHISHKUMAR M | Sath |
| 17 | 912020106018 | SIVANI S | |
| 18 | 912020106019 | SUJITHA B | Sujitha |
| 19 | 912020106020 | THILOTHAMA M | Thilo |
| 20 | 912020106021 | VALARMATHI S | |
| 21 | 912020106301 | ARUMUGAM | |
| 22 | 912020106302 | HARIVISHNU K | |

Course coordinator

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# STUDENTS ATTENDANCE

Pandian Saraswathi yadav Engineering College,Arasanoor -630561

Department of Electronics and Communication Engineering

**Student Attendance Sheet**

Academic Year : 2021-2022

Cource Code : VACECE2122VLSI

Course Name : VLSI Design using CADENCE Tools

Duration of hours : 35

Period of Course : 04.04.2022-08.04.2022

| Attendance Sheet | | | Date: 4/4/22 | | | | | |
|---|---|---|---|---|---|---|---|---|
| Sl. No | Register Number | Student Name | 09.00 am - 10.00 am | 10.00 am - 11.00 am | 11.15 am - 12.15pm | 01.00 pm - 02.00 pm | 02.00 pm - 03.00 pm | 03.15 pm - 04.15 pm |
| 1 | 912020106001 | AJAYKANNAN M | Ajk | Ajk | Ajk | Ajk | Ajk | Ajk |
| 2 | 912020106002 | ANITHA S | Anitha.s | Anitha.s | Anitha.s | Anitha.s | Anitha.s | Anitha.s |
| 3 | 912020106003 | ANTONY BRIGHTON N | Aron | Aron | Aron | Aron | Aron | Aron |
| 4 | 912020106004 | BHAVANI SRI G | bh | bh | bh | bh | bh | bh |
| 5 | 912020106006 | GOKULASUTHAN M | G.M | G.M | G.M | G.M | G.M | G.M |
| 6 | 912020106007 | GOWSALYA K | G | G | G | G | G | G |
| 7 | 912020106008 | KABILAN M | kabilan | kabilan | kabilan | kabilan | kabilan | kabilan |
| 8 | 912020106009 | KANIMOZHI D | D.kani | D.kani | D.kani | D.kani | D.kani | D.kani |
| 9 | 912020106010 | KARTHIKA V | V.k | V.k | V.k | V.k | V.k | V.k |
| 10 | 912020106011 | NANTHA KUMAR V | Nan | Nan | Nan | Nan | Nan | Nan |
| 11 | 912020106012 | NIVETHA T | Nivetha | Nivetha | Nivetha | Nivetha | Nivetha | Nivetha |
| 12 | 912020106013 | PREETHI VAASHINI M | Preethi | Preethi | Preethi | Preethi | Preethi | Preethi |
| 13 | 912020106014 | RANJITH P | Ranj | Ranj | Ranj | Ranj | Ranj | Ranj |
| 14 | 912020106015 | SARAN VP | Saran VP | Saran VP | Saran VP | Saran VP | Saran VP | Saran VP |
| 15 | 912020106016 | SARAVANAN K | Saravana | Saravana | Saravana | Saravana | Saravan | Saravana |
| 16 | 912020106017 | SATHISHKUMAR M | Sath | Sath | Sath | Sath | Sath | Sath |
| 17 | 912020106018 | SIVANI S | Si | Si | Si | Si | Si | Si |
| 18 | 912020106019 | SUJITHA B | Sujitha | Sujitha | Sujitha | Sujitha | Sujitha | Sujitha |
| 19 | 912020106020 | THILOTHAMA M | Thilo | Thilo | Thilo | Thilo | Thilo | Thilo |
| 20 | 912020106021 | VALARMATHI S | | | | | | |
| 21 | 912020106301 | ARUMUGAM | Arum | Arum | Arum | Arum | Arum | Arum |
| 22 | 912020106302 | HARIVISHNU K | Hari Vish | Hari Vish | Hari Vish | Hari Vish | Hari Vish | Hari Vish |

M. Dhiv

Course coordinator

R. Raj

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Pandian Saraswathi yadav Engineering College,Arasanoor -630561

Department of Electronics and Communication Engineering

Student Attendance Sheet

Academic Year : 2021-2022

Cource Code : VACECE2122VLSI

Course Name : VLSI Design using CADENCE Tools

Duration of hours : 35

Period of Course : 04.04.2022-08.04.2022

| Attendance Sheet | | | Date: 5/4/22 | | | | | |
|---|---|---|---|---|---|---|---|---|
| Sl. No | Register Number | Student Name | 09.00 am - 10.00 am | 10.00 am - 11.00 am | 11.15 am - 12.15pm | 01.00 pm - 02.00 pm | 02.00 pm - 03.00 pm | 03.15 pm - 04.15pm |
| 1 | 912020106001 | AJAYKANNAN M | | | | | | |
| 2 | 912020106002 | ANITHA S | | | | | | |
| 3 | 912020106003 | ANTONY BRIGHTON N | | | | | | |
| 4 | 912020106004 | BHAVANI SRI G | | | | | | |
| 5 | 912020106006 | GOKULASUTHAN M | | | | | | |
| 6 | 912020106007 | GOWSALYA K | | | | | | |
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| 13 | 912020106014 | RANJITH P | AB | AB | AB | AB | AB | AB |
| 14 | 912020106015 | SARAN VP | | | | | | |
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| 17 | 912020106018 | SIVANI S | | | | | | |
| 18 | 912020106019 | SUJITHA B | | | | | | |
| 19 | 912020106020 | THILOTHAMA M | | | | | | |
| 20 | 912020106021 | VALARMATHI S | AB | AB | AB | AB | AB | AB |
| 21 | 912020106301 | ARUMUGAM | | | | | | |
| 22 | 912020106302 | HARIVISHNU K | | | | | | |

Course coordinator

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Pandian Saraswathi yadav Engineering College,Arasanoor -630561

Department of Electronics and Communication Engineering

**Student Attendance Sheet**

Academic Year : 2021-2022

Cource Code : VACECE2122VLSI

Course Name : VLSI Design using CADENCE Tools

Duration of hours : 35

Period of Course : 04.04.2022-08.04.2022

| Attendance Sheet | | | Date: 6/4/22 | | | | | |
|---|---|---|---|---|---|---|---|---|
| Sl. No | Register Number | Student Name | 09.00 am - 10.00 am | 10.00 am - 11.00 am | 11.15 am - 12.15pm | 01.00 pm - 02.00 pm | 02.00 pm - 03.00 pm | 03.15 pm - 04.15 pm |
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Arasanoor, Thirumansolai P.O-630 561
Sivagangai Dist. Tamilnadu

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Pandian Saraswathi yadav Engineering College,Arasanoor -630561

Department of Electronics and Communication Engineering

**Student Attendance Sheet**

Academic Year : 2021-2022

Cource Code : VACECE2122VLSI

Course Name : VLSI Design using CADENCE Tools

Duration of hours : 35

Period of Course : 04.04.2022-08.04.2022

| Attendance Sheet | | | Date: 7/4/22 | | | | | |
|---|---|---|---|---|---|---|---|---|
| Sl. No | Register Number | Student Name | 09.00 am - 10.00 am | 10.00 am - 11.00 am | 11.15 am - 12.15pm | 01.00 pm - 02.00 pm | 02.00 pm - 03.00 pm | 03.15 pm - 04.15 pm |
| 1 | 912020106001 | AJAYKANNAN M | | | | | | |
| 2 | 912020106002 | ANITHA S | | | | | | |
| 3 | 912020106003 | ANTONY BRIGHTON N | | | | | | |
| 4 | 912020106004 | BHAVANI SRI G | | | | | | |
| 5 | 912020106006 | GOKULASUTHAN M | | | | | | |
| 6 | 912020106007 | GOWSALYA K | | | | | | |
| 7 | 912020106008 | KABILAN M | | | | | | |
| 8 | 912020106009 | KANIMOZHI D | | | | | | |
| 9 | 912020106010 | KARTHIKA V | | | | | | |
| 10 | 912020106011 | NANTHA KUMAR V | AB | AB | AB | AB | AB | AB |
| 11 | 912020106012 | NIVETHA T | | | | | | |
| 12 | 912020106013 | PREETHI VAASHINI M | | | | | | |
| 13 | 912020106014 | RANJITH P | | | | | | |
| 14 | 912020106015 | SARAN VP | | | | | | |
| 15 | 912020106016 | SARAVANAN K | AB | AB | AB | AB | AB | AB |
| 16 | 912020106017 | SATHISHKUMAR M | | | | | | |
| 17 | 912020106018 | SIVANI S | | | | | | |
| 18 | 912020106019 | SUJITHA B | | | | | | |
| 19 | 912020106020 | THILOTHAMA M | | | | | | |
| 20 | 912020106021 | VALARMATHI S | | | | | | |
| 21 | 912020106301 | ARUMUGAM | | | | | | |
| 22 | 912020106302 | HARIVISHNU K | | | | | | |

Course coordinator

HOD/ECE

PRINCIPAL

PRINCIPAL
PANDIAN SARASWATHI YADAV
ENGINEERING COLLEGE
Arasanoor, Thirumansolai P.O-630 561
Sivagangai Dist. Tamilnadu

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Pandian Saraswathi yadav Engineering College,Arasanoor -630561

Department of Electronics and Communication Engineering

## Student Attendance Sheet

Academic Year : 2021-2022

Cource Code : VACECE2122VLSI

Course Name : VLSI Design using CADENCE Tools

Duration of hours : 35

Period of Course : 04.04.2022-08.04.2022

| Attendance Sheet | | | Date: 8/4/22 | | | | | |
|---|---|---|---|---|---|---|---|---|
| Sl. No | Register Number | Student Name | 09.00 am - 10.00 am | 10.00 am - 11.00 am | 11.15 am - 12.15pm | 01.00 pm - 02.00 pm | 02.00 pm - 03.00 pm | 03.15 pm - 04.15 pm |
| 1 | 912020106001 | AJAYKANNAN M | | | | | | |
| 2 | 912020106002 | ANITHA S | | | | | | |
| 3 | 912020106003 | ANTONY BRIGHTON N | | | | | | |
| 4 | 912020106004 | BHAVANI SRI G | | | | | | |
| 5 | 912020106006 | GOKULASUTHAN M | | | | | | |
| 6 | 912020106007 | GOWSALYA K | | | | | | |
| 7 | 912020106008 | KABILAN M | | | | | | |
| 8 | 912020106009 | KANIMOZHI D | | | | | | |
| 9 | 912020106010 | KARTHIKA V | | | | | | |
| 10 | 912020106011 | NANTHA KUMAR V | | | | | | |
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| 15 | 912020106016 | SARAVANAN K | | | | | | |
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| 17 | 912020106018 | SIVANI S | | | | | | |
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Course coordinator

HOD/ECE

PRINCIPAL

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Arasanoor, Thirumansolai P.O-630 561
Sivagangai Dist. Tamilnadu

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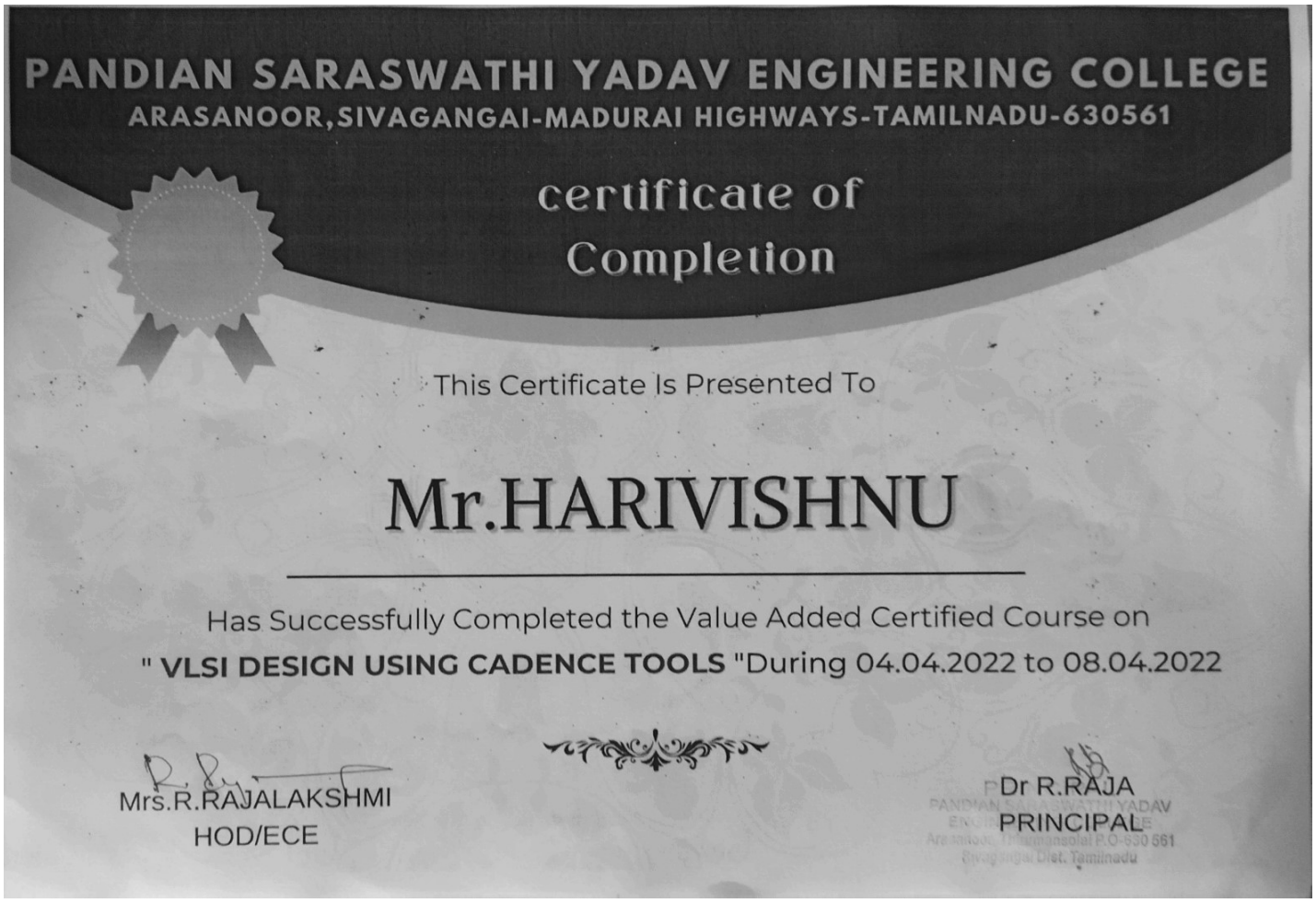
# MODEL CERTIFICATES

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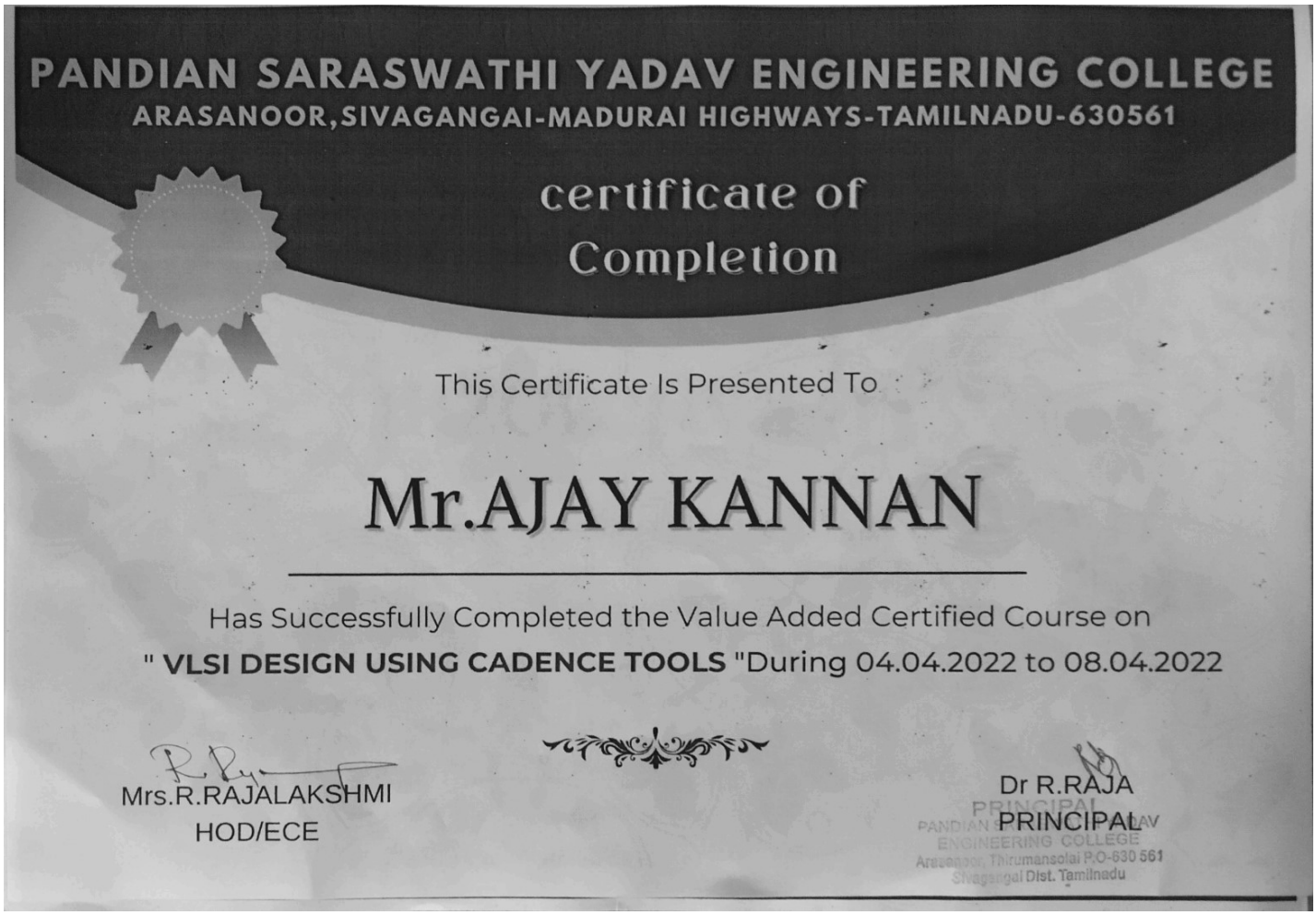

PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

ARASANOOR,SIVAGANGAI-MADURAI HIGHWAYS-TAMILNADU-630561

certificate of Completion

This Certificate Is Presented To

Mr.AJAY KANNAN

Has Successfully Completed the Value Added Certified Course on

" **VLSI DESIGN USING CADENCE TOOLS** "During 04.04.2022 to 08.04.2022

Mrs.R.RAJALAKSHMI
HOD/ECE

Dr R.RAJA
PRINCIPAL

PRINCIPAL
PANDIAN SARASWATHI YADAV
ENGINEERING COLLEGE
Arasanoor, Thirumansolai P.O-630 561
Sivagangai Dist. Tamilnadu

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# PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE

ARASANOOR,SIVAGANGAI-MADURAI HIGHWAYS-TAMILNADU-630561

## certificate of Completion

This Certificate Is Presented To

# Ms.KANIMOZHI

Has Successfully Completed the Value Added Certified Course on

" **VLSI DESIGN USING CADENCE TOOLS** "During 04.04.2022 to 08.04.2022

Mrs.R.RAJALAKSHMI
HOD/ECE

Dr R.RAJA
PRINCIPAL

PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE Arasanoor, Thirumansolai P.O-630 561 Sivagangai Dist. Tamilnadu

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