**PANDIAN SARASWATHI YADAV ENGINEERING COLLEGE**

 **DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING**

**ACADEMIC YEAR: 2016- 2017 / ODD SEMESTER**

**SUBJECT CODE: EE6301**

**SUBJECT NAME: DIGITAL LOGIC CIRCUITS**

**YEAR / SEM: II / III**

**FACULTY INCHARGE: S.PANDIMEENA**

**QUESTION BANK**

**UNIT I -NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES**

**1) What are basic properties of Boolean algebra? NOV/DEC2008**

**2) State the associative property of boolean algebra. NOV/DEC2008**

**3) State the commutative property of Boolean algebra**.APRIL/MAY2008

**4) State the distributive property of Boolean algebra.** APRIL/MAY2008

**5) State the absorption law of Boolean algebra**. **NOV/DEC2009**

**6) State De Morgan's theorem.NOV/DEC2009**

**7) Reduce A (A + B).** APRIL/MAY2009

**8) Reduce A'B'C' + A'BC' + A'BC.** APRIL/MAY2009

**9) Reduce AB + (AC)' + AB’C (AB + C) NOV/DEC2010**

**10) Simplify the following expression Y = (A + B) (A + C’) (B' + C’**) Y **NOV/DEC2010**

**11) Show that (X + Y' + XY)=0.APR/MAY2010**

**12) Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC. APR/MAY2010**

**13) Convert the given expression in canonical SOP form Y = AC + AB + BC. NOV/DEC2011**

**14) Define duality property**. **NOV/DEC2011**

**PART:B**

**1. Discuss about TTL parameters. NOV/DEC2008**

**2. Draw and explain the circuit diagram of CMOS NOR gate. NOV/DEC2008**

**3. Name and explain the characteristics of TTL family.** APRIL/MAY2008

**4. Explain the characteristics and implementation of the following digital logic families.**

 **(a) CMOS (b) ECL (c) TTL** APRIL/MAY2008,

**5.Describe the concept working and applications of the following memories:**

 **(a)PLD(b)FPGA(c)EPROM , APR/MAY2010**, APRIL/MAY2009

**6. Explain the classifications of binary codes. NOV/DEC2010, APR/MAY2010**

**7. Explain about error detection and correction codes . NOV/DEC2011, APR/MAY2010**

**UNIT II -COMBINATIONAL CIRCUITS**

**1. What are the classifications of sequential circuits? NOV/DEC2008**

**2. Define Flip flop. NOV/DEC2008**

**3. What are the different types of flip-flop?** APRIL/MAY2008

**4. What is the operation of RS flip-flop?** APRIL/MAY2008

**5. What is the operation of SR flip-flop? NOV/DEC2009**

**6. What is the operation of D flip-flop? NOV/DEC2009**

**7. What is the operation of JK flip-flop?** APRIL/MAY2009

**8. What is the operation of T flip-flop?** APRIL/MAY2009

**9. Define race around condition. NOV/DEC2010**

**10. What is edge-triggered flip-flop? NOV/DEC2010**

**11. What is a master-slave flip-flop?** APRIL/MAY2010

**12. Explain the flip-flop excitation tables for RS FF.** APRIL/MAY2010

**13. Explain the flip-flop excitation tables for JK flip-flop NOV/DEC2011**

**14. Explain the flip-flop excitation tables for D flip-flop NOV/DEC2011**

**PART B**

**1. Obtain the minimum SOP using QUINE- McCLUSKY method and verify using K-map F=m0+m2+m4+m8+m9+m10+m11+m12+m13 NOV/DEC2008**

**2. Reduce the following using tabulation method. NOV/DEC2008**

**3. F=m2+m3+m4+m6+m7+m9+m11+m13.** APRIL/MAY2008

**4. Reduce the Boolean function using k-map technique and implement using gates f (w, x, y, z)= Σm (0,1,4,8,9,10) which has the don’t cares condition**

**d (w, x, y, z)= Σm (2,11).** APRIL/MAY2008

**5. (a)Design an 8421 to gray code converter. (b)Implement the Boolean function using 8:1 mux F (A, B, C, D) =A’BD’+ACD+B’CD+A’C’D. NOV/DEC2009**

**6. Design A Full Adder And A Full Subtractor. NOV/DEC2009**

**7. A combinational circuit is defined by the following three Boolean functions F1 = x’y’z’+xz F2= xy’z’+x’y F3= x’y’z+xy. Design the circuit with a decoder and**

**external gates. NOV/DEC2010**

**8. Simplify the following Boolean function by using Tabulation method F (w, x, y, z) =Σm (0, 1, 2, 8, 10, 11, 14, 15)** APRIL/MAY2009

**9. Simplify the following Boolean functions by using K’Map in SOP & POS.**

 **F (w, x, y, z) = Σm (1, 3, 4, 6, 9, 11, 12, 14)** APRIL/MAY2010

**10. (a) Design a 2 bit magnitude comparator. (b) Explain the operation of**

 **4 to 10 decoder.** APRIL/MAY2011

**UNIT III -SYNCHRONOUS SEQUENTIAL CIRCUITS**

**1. What are secondary variables?** APRIL/MAY2008

**2. What are excitation variables?** APRIL/MAY2008

**3. What is fundamental mode sequential circuit? NOV/DEC2008**

**4. What is pulse mode circuit? NOV/DEC2008**

**5. What is non critical race?** APRIL/MAY2009

**6. What is critical race?** APRIL/MAY2009

**7. When does a cycle occur? NOV/DEC2009**

**8. What are the different techniques used in state assignment? NOV/DEC2009**

**9. What are the steps for the design of asynchronous sequential circuit?** APRIL/MAY2010

**10. What is hazard?** APRIL/MAY2010

**11. What is static 1 hazard? NOV/DEC2010**

**12. What are static 0 hazards? NOV/DEC2010**

**13. What is dynamic hazard?** APRIL/MAY2011

**14.What is the cause for essential hazards?** APRIL/MAY2011

**PART B**

**1. A sequential circuit has 2D ff’s A and B an input x and output y is specified by the following next state and output equations. a. A (t+1)= Ax + Bx , NOV/DEC2009**

 **b. B (t+1)= A’x c. Y= (A+B) x’**

**(i) Draw the logic diagram of the circuit.**

**(ii) Derive the state table.**

**(iii) Derive the state diagram.**

**2. Design a mod-10 synchronous counter using Jk ff. write excitation table and**

 **state table. NOV/DEC2009**

**3. a) Write the excitation tables of SR, JK, D, and T Flip flops (b) Realize D and T flip flops using Jk flip flops ,** APRIL/MAY2011

**4. Design a sequential circuit using JK flip-flop for the following state table**

 **[use state diagram]** APRIL/MAY2011

**5. Design a counter with the following repeated binary sequence:0, 1, 2, 3, 4, 5, 6.use JK Flip-flop. NOV/DEC2010**

**6. Design a 3 bit synchronous gray code counter using flip flop. NOV/DEC2010**

**7. Draw and explain the block diagram of Mealy circuit.** APRIL/MAY2010

**8. Using positive edge triggering SR flip-flops design a counter which counts in the**

 **following sequence: 000,111,110,101,100,011,010,001,000,…** APRIL/MAY2010

**UNIT IV- ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE LOGIC DEVICES**

**1. Explain ROM** APRIL/MAY2008

**2. What are the types of ROM?** APRIL/MAY2008

**3. Explain PROM.** **NOV/DEC2008**

**4. Explain EPROM. NOV/DEC2008**

**5. Explain EEPROM**. APRIL/MAY2009

6**. Define address and word,** APRIL/MAY2009

**7. What are the types of ROM.? NOV/DEC2009**

**8. What is programmable logic array? How it differs from ROM? NOV/DEC2009**

**9. What is mask - programmable?** APRIL/MAY2010

**10. What is field programmable logic array?** APRIL/MAY2010

**11. List the major differences between PLA and PAL, NOV/DEC2010**

**12. Define PLD. NOV/DEC2010**

**13. Give the classification of PLDs.** APRIL/MAY2011

**14. Define PROM.** APRIL/MAY2011

**PART B**

**1. Design an asynchronous sequential circuit that has 2 inputs x2 and x1, and one output z. the output is to remain 0 as long as an X1 is 0. The first change in x2 that occurs while x1 is 1 will cause z to be 1. Z is to remain 1 until x1 returns to 0.**

**Construct a state diagram and flow table. Determine the output equations. NOV/DEC2008**

**2. Design a circuit with inputs A and B to give an output z=1 when AB=11 but only if A becomes 1 before B, by drawing total state diagram, primitive flow table and output map in which transient state is included NOV/DEC2008**

**3. Obtain the primitive flow table for an asynchronous circuit that has** APRIL/MAY2008

**2 input’s x, y and output z. an output z=1, is to occur only during the input state xy=01 and then if and only if the input state xy=01 is preceded by the input sequence**

 **xy=01, 00, 10, 00, 10, 00 ,**

**4. Design a circuit with input a and b to give an output z=1 when AB =11 but only if A becomes 1 before B, by drawing total state diagram, primitive flow table and**

**output map in which transient state is included.** APRIL/MAY2008

**5. Design a asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T = 1 & c moves from 1 to 0. Otherwise the output is 0. NOV/DEC2009**

**6. Design an Asynchronous sequential circuit using SR latch with two inputs A and B and one output y. B is the control input which, when equal to 1, transfers the input A to output y. when B is 0, the output does not change, for any change in input NOV/DEC2009**

**7. a. Explain the difference between synchronous and asynchronous sequential circuits. b. Derive the transition table for the asynchronous sequential circuit shown below. Determine the sequence of internal states Y1Y2 for the following sequence of inputs**

 **x1x2 : 00,10,11,01,11,10,00.** APRIL/MAY2009

**8. Derive the transition table and logic diagram for an asynchronous sequential circuit with the help of the following flow table.** APRIL/MAY2009

**9. a) Explain in detail about PLA with a specific example. b) Explain with neat diagrams RAM architecture NOV/DEC2010**

**10. Implement the following function using PLA. a. A (x, y, z) = Σm (1, 2, 4, 6) NOV/DEC2010**

**b. B (x, y, z) = Σm (0, 1, 6, 7)**

**c. C (x, y, z) = Σm (2, 6)**

**UNIT V -VHDL**

**1. What is Verilog?** APRIL/MAY2008

**2. What are the various modeling used in Verilog?** APRIL/MAY2008

**3. What is the structural gate-level modeling? NOV/DEC2008**

**4. What is Switch-level modeling? NOV/DEC2008**

**5. What are identifiers?** APRIL/MAY2009

**6. What are the value sets in Verilog?** APRIL/MAY2009

**7. What are the types of gate arrays in ASIC? NOV/DEC2009**

**8. What are gate primitives? NOV/DEC2009**

**9. Give the two blocks in behavioral modeling.** APRIL/MAY2010

**10. What are the types of procedural assignments?** APRIL/MAY2010

**11.Give theclassifications oftimingcontrol. NOV/DEC2010**

**12 .Give the different arithmetic operators? NOV/DEC2010**

**13. Give the different bitwise operators.** APRIL/MAY2011

**14. What are the types of conditional statements?** APRIL/MAY2011

**PART B**

**1. Write a HDL code for state machine to BCD to ex–3 codes Converter.** APRIL/MAY2008

**2. Write a behavioral VHDL description of an S-R latch using a process** APRIL/MAY2008

**3. Write a HDL code for 8:1 MUX using behavioral model NOV/DEC2009**

**4. Write the HDL description of the circuit specified by the Following Boolean equations**

 **a. S = xy ‘+ x’ y NOV/DEC2009**

 **b. C =xy**

**5.Write an HDL data flow description of a 4 bit adder subtractor of Unsigned numbers use the conditional operator** APRIL/MAY2009

**6.Write the HDL gate level description of the priority encoder** APRIL/MAY2009

**7.Write VHDL code for a full sub tractor using logic Equation NOV/DEC2010**

**8.Write a VHDL description of an S-R latch using a process. NOV/DEC2010**